AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An array substrate for a liquid crystal display device, comprising:

a substrate;

gate and data lines crossing each other on the substrate;

a thin film transistor connected to the gate and data lines, the thin film transistor having a gate electrode, a semiconductor layer, and source and drain electrodes facing and spaced apart from each other;

a passivation layer over the gate and data lines and the thin film transistor, the passivation layer having a contact hole exposing a portion of a side surface of the drain electrode;

a gate insulation layer formed underneath the passivation layer, wherein the contact hole is defined through the passivation layer and the gate insulation layer;

a pixel electrode on the passivation layer; and

a storage capacitor including a portion of the gate line as a first storage electrode, a portion of the gate insulation layer, and a second storage electrode having an island shape, ~~wherein the first storage electrode is formed of the same material as the gate electrode and the second storage electrode is formed of the same material as the source and drain electrodes and disposed on the gate insulation layer~~ wherein the second storage electrode is disposed directly contacting the gate insulation layer.

2. (Previously Presented) The array substrate according to claim 1, wherein the pixel electrode is electrically connected to the drain electrode through the contact hole, and also contacts the substrate through the contact hole.

3. (Canceled)

4. (Canceled)

5. (Original) The array substrate according to claim 1, wherein the contact hole further exposes a portion of a top surface of the drain electrode.

6. (Previously Presented) An array substrate for a liquid crystal display device, comprising:

a substrate;

gate and data lines crossing each other on the substrate;

a thin film transistor connected to the gate and data lines, the thin film transistor having a gate electrode extending from the gate line, a semiconductor layer, a first ohmic contact layer, a second ohmic contact layer, and source and drain electrodes, the semiconductor layer having an end aligned with and directly below an end of the source electrode, the semiconductor layer having an opposite end aligned with and directly below an end of the drain electrode;

a passivation layer pattern on the data line and the thin film transistor, the passivation layer pattern exposing a portion of a side surface of the drain electrode; and

a pixel electrode connected to the drain electrode; and

a gate insulation film formed over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film at a pixel region defined by the gate and data lines.

7. (Currently Amended) The array substrate according to claim 6, further comprising a storage capacitor including a first storage electrode, a portion of a gate insulation layer, and a second storage electrode, ~~wherein the first storage electrode is formed of the same material as the gate electrode and the second storage electrode is formed of the same material as the source and drain electrode,~~ and wherein the pixel electrode contacts the second storage electrode through a contact hole formed through the passivation layer.

8. (Previously Presented) The array substrate according to claim 6, wherein the first ohmic contact layer has an end aligned with and directly below the end of the source electrode and the second ohmic contact layer has an end aligned with and directly below the end of the drain electrode.

9. (Previously Presented) The array substrate according to claim 6, wherein the passivation layer pattern exposes a portion of only one side surface of the drain electrode.

10. (Canceled)

11. (Original) The array substrate according to claim 6, wherein the passivation layer pattern further exposes a portion of a top surface of the drain electrode.

12. (Currently Amended) An array substrate for a display device, comprising:

a substrate;

a gate line on the substrate;

a gate insulator on the gate line;

a semiconductor layer on the gate insulator;

a first ohmic contact layer and a second ohmic contact layer on the semiconductor layer;

a data line and source and drain electrodes on the plurality of ohmic contact layers, the source electrode connected to the data line, the drain electrode facing and spaced apart from the source electrode;

a passivation layer on the source and drain electrodes and covering a crossing portion of the gate and data lines, a portion of a side surface of the drain electrodes being exposed;

a pixel electrode connected to the drain electrode~~,~~;

~~wherein the gate insulator comprises a gate insulation film formed over the gate line,~~ wherein a portion of the pixel electrode is formed directly ~~on~~ contacting the gate ~~insulation film~~ insulator at a pixel region defined by the gate and data lines,

wherein the pixel electrode contacts side portions of the semiconductor layer and one of the first and second ohmic layers.

wherein the first ohmic contact layer has an end aligned with and directly below an end of the source electrode and the second ohmic contact layer has an end aligned with and directly below an end of the drain electrode, and

wherein the semiconductor layer has an end aligned with and directly below the end of the source electrode, and an opposite end aligned with and directly below the end of the drain electrode.

13. (Canceled).

14. (Previously Presented) The array substrate according to claim 12, wherein the passivation layer exposes a portion of a top surface of the drain electrode.

15-21 (Canceled)

22. (Currently Amended) The array substrate according to claim 12, further comprising a storage capacitor including a first storage electrode, a portion of the gate insulator, and a second storage electrode, wherein the pixel electrode contacts the second storage electrode through a contact hole formed through the passivation layer~~, and wherein the first storage electrode is formed of the same material as the gate electrode and the second storage electrode is formed of the same material as the source and drain electrodes~~.